REMARKS/ARGUMENTS

Claims 1-24 remain pending in this application. Claims 25-34 are canceled. Claims 1, 6 and 8-9 stand rejected under 35U.S.C. 102(b) as being anticipated by Yamano. Claims 2-5 and 7 are objected to as being dependent upon a rejected claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 10-24 are allowed.

In rejecting claim 1, the Examiner asserts:

> Yamano in Figures 8-11 disclosed a non-volatile memory (101, Figure 9) comprising:
> a nonvolatile memory element (104, Figure 9) having at least first and second terminal;
> a voltage source (example, the voltage between 7-9 volts applied to the drain and the source which generate the hot electron in Figure 8, see column 1, lines 57-61) coupled to at least one terminal to provide a first voltage during a first time period being less than the voltage required (threshold voltage 12 voltage, Figure 8) for electrons to flow to or from a floating gate of the nonvolatile memory element (see column 1, lines 51-67) and
> a charge pump circuit(107, Figure 9-10) couple to at least one terminal including at least one capacitor (the charge pump 107 in Figure 10 include a capacitor 114, 155) that receives a second voltage (the charge pump 107 is supply with a power supply Vcc(113) in Figure 100) during a second time period increase the voltage on the terminal that the electrode flow or floating gate of the nonvolatile memory element (example, see column 2, lines 58 through column 3, lines 6).

Applicants respectfully traverse this rejection. Fig. 8 of Yamano is a schematic diagram showing electrical connections during operation in a typical structure of a memory cell in a flash memory (1:22-24). Yamano further provides:

> In order to write data, in the case of an ordinary flash memory using hot electrons, a voltage as high as about +12 V is applied to the control gate CG and the source S is grounded in the state where data is erased, as shown in FIG. 8. At the same time, a voltage of about +7 to +9 V or 0 V depending on the data to be written is applied to the drain D. At this time, when a voltage of about +7 to +9 V is applied to the drain D, a

> large drain current flows between the drain D and the source S, and generates hot electrons. The thus generated hot electrons having high energy are injected to the floating gate FG. On the other hand, in the case where the drain D is grounded (i.e., a voltage of 0 V is applied to the drain D), the electron injection by hot electrons is not performed. Thus, whether the electron injection to the floating gate FG is performed or not can be controlled in accordance with a voltage applied to the drain D. This makes it possible to write data in the flash memory. (1:51-67)

Fig. 9 shows, among other things, a flash memory 101 and a charge pump circuit 107:

> In FIG. 9, a flash memory 101 is connected to a CPU 102 for controlling the system via a bus line 103. A peripheral 112 and other various devices (not shown in FIG. 9) are connected to the bus line 103 via an I/O port 111. The flash memory 101 includes therein a memory cell array 104, a command judging circuit 105 and a charge pumping circuit 107 therein. (2:18-24)

Fig. 10 is a circuit schematic diagram of charge pump 107, whose operation is described in columns 2, lines 40-67; and column 3. In particular, Yamano provides:

> ....The charge pumping circuit 107 is supplied with a power supply voltage Vcc... (2:42-43)
>
> ....As a result, a voltage twice as high as the power supply voltage Vcc at the maximum can be obtained from the output terminals 120..... (3:4-6)

> ....The high voltage output from the charge pumping circuit 107 described above is supplied to the memory cell array 104 as shown in FIG. 9, so as to conduct the data-writing operation or the erasing operation. Therefore, in the flash memory 101, the data-writing operation or the erasing operation can be performed as a result of internally generating the high voltage in the flash memory by simply supplying the power supply voltage Vcc corresponding to the reference voltage of the apparatus.....(3:29-37)

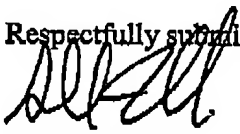
In other words, as best understood, the high voltages required by the memory shown in Fig. 8 of Yamano is provided by charge pump circuit shown in Fig. 10 of Yamano. However, there is no

disclosure in Yamano that a voltage provided to at least one terminal of the non-volatile memory element during a first time period, and being less than the voltage required for the electrons to flow to or from a floating gate of the non-volatile memory element, is increased during a second time period by a charge pump that includes at least one capacitor, and such that the electrons flow to or from the floating gate of the non-volatile memory element, as required in claim 1. The Examiner refers to the 7-9 volts that is applied to the drain and the source of the memory as the first voltage, and the VCC voltage received by the charge pump as the second voltage. However, there is no disclosure in Yamano that the 7-9 volts applied to the drain and the source of the memory during a first time period is increased by the charge pump in accordance with the second voltage, Vcc, during a second time period, as required by claim 1. If the Examiner believes otherwise, the Examiner is respectfully requested to show "said first voltage being less than the voltage required to for electrons to flow to or from a floating gate of the nonvolatile memory element", and to further show that "the charge pump circuit ..... receives a second voltage during a second time period, and in accordance therewith, further increases the voltage on said terminal so that electrons flow to or from the floating gate of the nonvolatile memory element." Claim1 and its dependent claims 2-9 are thus allowable over Yamano for at least the above reasons.

In view of the foregoing, Applicants believe all claims, namely claims 1-24, now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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